1   1.   A method for determining a specification of a

2   synchronous digital circuit comprising:

3   accepting a first specification of a first

4   asynchronous digital system, including accepting a

5   specification of a plurality of data elements whose values

6   define the state of the system and a first plurality of

7   state transition rules for the asynchronous digital system;

8   and

9   determining a specification of a synchronous digital

10   circuit from the specification of the asynchronous digital

11   system, wherein during at least some clocking periods the

12   synchronous digital circuit makes a state transition

13   equivalent to state transitions specified by a plurality of

14   the state transition rules specified for the asynchronous

15   digital system.

1   2.   The method of claim 1 wherein each state

2   transition rule includes a specification of a precondition

3   that must be satisfied by the state of the system to apply

4   the state transition rule, and a specification of a

5   resulting state that is reached as a result of applying the

6   state transition rule.

1   3.   The method of claim 2 wherein the state

2   transition rules are defined as a term rewriting system.

1   4.   The method of claim 3 wherein the specification
2 of the synchronous digital system is in a register transfer
3 language.

1   5.   The method of claim 1 further comprising
2 scheduling the state transition rules including identifying
3 one or more sets of conflicting state transition rules for
4 which state transitions specified by different rules in one
5 of the conflicting sets may conflict in their access to
6 data elements of the system.

1   6.   The method of claim 5 wherein determining the
2 specification of the synchronous system includes
3 determining said specification such that during any
4 clocking period, the synchronous digital circuit makes
5 states transitions equivalent to at most one state
6 transition rule from each conflicting set of state
7 transition rules.

1   7.   The method of claim 6 wherein determining the
2 specification of the synchronous system includes
3 determining a specification of arbitration logic associated
4 with each conflicting set of state transition rules such
5 that the arbitration logic generates trigger signals that
6 allow at most one state transition rule from the
7 conflicting set of states to be applied in a single
8 clocking period.

1   8.   The method of claim 7 wherein the arbitration
2 logic includes a round-robin priority encoder for
3 generating the trigger signals.

1   9.   The method of claim 1 further wherein determining
2 the specification of the synchronous system includes
3 determining a specification of arbitration logic that
4 generates trigger signals for sets of state transitions
5 rules such that the rules in each of said are applicable in
6 at least some order to the asynchronous digital system.

1   10. The method of claim 1 further comprising:
2   transforming the first specification of the first
3 asynchronous digital system into a second specification of
4 a second asynchronous digital system, wherein the second
5 specification includes a second plurality of state
6 transition rules, and the second asynchronous digital
7 system includes pipeline;
8   wherein at least some of the first state transitions
9 rules each correspond to a plurality of the second state
10 transition rules such that each of these corresponding
11 rules of the second plurality of state transition rules is
12 associated with a different stage of the pipeline.

1   11. The method of claim 1 further comprising:

2   adding a plurality of composite rules to the first

3   specification, wherein each composite rule is associate

4   with a plurality of the first state transition rules, and

5   each state transition specified by one of the composite

6   state transition rules is equivalent to a sequence of state

7   transitions each specified by the first plurality of state

8   transition rules.

1   12. The method of claim 1 wherein accepting the

2   specification of the data elements further includes

3   accepting a specification of an abstract data type, and

4   wherein determining a specification of a synchronous

5   digital circuit includes determining an implementation of

6   the abstract data type.

1   13. The method of claim 12 wherein the abstract data

2   type is a first-in-first-out queue, and the implementation

3   of the abstract data type is a register.

1   14. The method of claim 1 wherein the synchronous

2   digital circuit implements a computer processor, and state

3   transitions of the asynchronous digital system are

4   associated with changes in values stored in storage

5   elements of the computer processor.

1   15. The method of claim 1 wherein determining the
2 specification of the synchronous circuit further includes
3 determining a preliminary specification of a digital
4 circuit, and optimizing the preliminary specification a
5 correspondence between the preliminary specification and
6 the specification of the asynchronous digital system.

1   16. A method for determining a specification an
2 asynchronous digital system comprising:
3   accepting a first specification of a first
4 asynchronous digital system, including accepting a
5 specification of a plurality of data elements whose values
6 define the state of the system and a first plurality of
7 state transition rules for the asynchronous digital system;
8   transforming the first specification of the first
9 asynchronous digital system into a second specification of
10 a second asynchronous digital system, wherein the second
11 specification includes a second plurality of state
12 transition rules, and the second asynchronous digital
13 system includes pipeline;
14   wherein at least some of the first state transitions
15 rules each correspond to a plurality of the second state
16 transition rules such that each of these corresponding
17 rules of the second plurality of state transition rules is
18 associated with a different stage of the pipeline.

1   17. The method of claim 1 further comprising:

2   adding a plurality of composite rules to the first

3 specification, wherein each composite rule is associate

4 with a plurality of the first state transition rules, and

5 each state transition specified by one of the composite

6 state transition rules is equivalent to a sequence of state

7 transitions each specified by the first plurality of state

8 transition rules.

1   18. A method for specifying a digital circuit
2   implementing an instruction set architecture for a computer
3   processor comprising:
4   accepting a first specification of a first
5   asynchronous digital system which implements the
6   instruction set architecture, including accepting a first
7   plurality of state transition rules, each rule specifying a
8   classes of state transitions of the asynchronous digital
9   system and including a specification of a precondition that
10   must be satisfied to apply the state transition rule, and a
11   specification of a resulting state that is reached as a
12   result of applying the state transition rule;
13   transforming the first specification into a second
14   specification of a second asynchronous digital system,
15   wherein the second specification includes a second
16   plurality of state transition rules, and the second
17   asynchronous digital system includes pipeline, wherein at
18   least some of the first state transitions rules each
19   correspond to a plurality of the second state transition
20   rules such that each of these corresponding rules of the
21   second plurality of state transition rules is associated
22   with a different stage of the pipeline;
23   adding a plurality of composite rules to the second
24   specification, wherein each composite rule is associate
25   with a plurality of the second state transition rules, and
26   each state transition specified by the composite state
27   transition rule is equivalent to a sequence of two state
28   transitions each specified by the second plurality of state
29   transition;

30   determining a specification of a synchronous digital

31   circuit from the specification of the asynchronous digital

32   system and the identified sets of conflicting state

33   transition rules, wherein during at least some clocking

34   periods, the synchronous digital circuit makes a state

35   transition equivalent to state transitions specified by a

36   plurality of state transition rules.

1   19.   Software stored on a computer-readable medium for

2   causing a computer to perform the functions of:

3   accepting a first specification of a first

4   asynchronous digital system, including accepting a

5   specification of a plurality of data elements whose values

6   define the state of the system and a first plurality of

7   state transition rules, each state transition rule

8   specifying a classes of state transitions of the

9   asynchronous digital system;

10   scheduling the state transition rules including

11   identifying sets of state transition rules that can be

12   applied concurrently without conflict; and

13   determining a specification of a synchronous digital

14   circuit from the specification of the asynchronous digital

15   system, wherein during at least some clocking periods the

16   synchronous digital circuit makes a state transition

17   equivalent to state transitions specified by a plurality of

18   the state transition rules specified for the asynchronous

19   digital system.